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Metal-Oxide-Semiconductor Transistors and their Applications

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The characteristics and mode of operation of m-o-s transistors are discussed. Uses of the devices in choppers, impedance converters, and other applications including voltage controlled resistors, are treated practically and mathematically. Practical circuits are given.

INTRODUCTION

This article is intended to serve as an introduction to engineers who are interested in the applications in which the Mullard BSX82 and BFX63 metal-oxide-semiconductor transistors, which are now in quantity production, can be used.

The m-o-s transistor is an insulated-gate field-effect device; the insulation is achieved by means of a silicon dioxide dielectric. It is well suited for use in impedance converters that require a high input impedance, and because it has a negligible offset voltage it is particularly suitable for use as a chopper transistor, and as a voltage variable resistor, for example in variable gain amplifiers.

The m-o-s transistor is a majority carrier device with negligible transit time effects, unlike more conventional transistors. Hence, the performance at high frequencies is, in general, limited only by capacitance.

DESCRIPTION AND OPERATION

The BSX82 and BFX63 metal-oxide-semiconductor transistors consist of two diffused, very rich n regions (or n+ regions) on a p-type silicon substrate as shown in Fig. 1. The symbols for the transistor and its electrodes are as shown in Fig. 2. The n+ regions, which are known as the 'source' and the 'drain', are close together. On the substrate between them, a thin layer of silicon dioxide acts as a dielectric between the substrate and an aluminium electrode called the 'gate'.

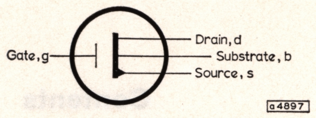


Fig. 2—Graphical symbol used in this article for m-o-s transistor

When the gate is made positive with respect to the source, holes will be repelled from, and electrons attracted to, the surface of the substrate. Consequently, an n-type layer is formed in the substrate near the oxide dielectric. The greater the applied potential, the thicker will be this inversion layer. The inversion layer forms a conducting path, therefore current will flow between the n+ regions if a potential is applied between the drain and the source. Because it controls the thickness of the inversion layer, the gate voltage also controls the resistance between the drain and source (r_{DS}) in the chopper mode, or the drain current in the amplifying mode.

As the substrate region under the gate is not of uniform material it may be made with an intrinsic inversion layer and a negative gate voltage is required to remove this; alternatively, if the material is rich in holes a positive gate voltage is required before the inversion layer can start to form. This gate voltage, which is defined for simplicity of measurement as the gate voltage to produce an arbitrary very low drain current (20μA), is known as the pinch-off or cut-off voltage $V_{(P)GS}$.

The BSX82 and BFX63 m-o-s transistors are four-terminal devices with an input capacitance of 5pF, an input resistance exceeding $10^{11}\Omega$, a mutual conductance exceeding 1·3mA/V at 5mA drain current, and a negative cut-off voltage between 0 and −4·5V.

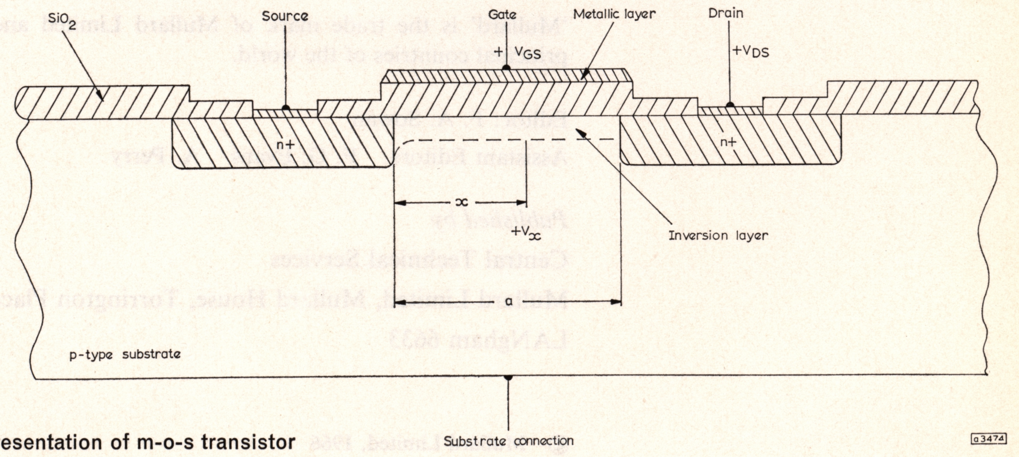


Fig. 1—Diagrammatic representation of m-o-s transistor

BSX82 TRANSISTOR AS A CHOPPER

The chopper transistor may be characterised by five parameters: offset voltage, offset current, ON and OFF resistances, and spike feedthrough; and by the thermal coefficient and drift with time of each of these parameters. The following sections consider each of the above parameters except spike feedthrough, which will be dealt with later under *Simple Chopper*.

Offset Voltage

The offset voltage appears during the ON (short circuit) state of a chopper transistor and is independent of the d.c. input voltage. It therefore constitutes a zero error. If it is backed off by a constant voltage, an error remains because of the change of offset voltage with time and temperature.

In the BSX82 the conduction path is an n-type channel between n+ type contacts, and is a pure resistance. The only offset voltage generated is due to the thermal effects and contact potentials between internal connections. Offset voltages, negligible compared with the 0·1 to 2mV typical of bipolar transistors and temperature coefficients much smaller than 1μV/degC, obtained in bipolar transistors, are now possible.

Offset Current

The offset current appears during the OFF (high resistance) state of the chopper, and is due to the feedthrough of the switching voltage into the output. In the bipolar transistor the feedthrough path is the reverse biased collector-emitter diode which may give 1nA with 1V switching signal at 25°C, increasing exponentially with temperature. In the m-o-s transistor the feedthrough path is the silicon oxide layer. Any surface leakage on the header will be 'guarded' by the envelope, which is connected to substrate and normally to source. A typical value for this leakage resistance would be $10^{12}\Omega$, and it does not decrease significantly with increasing temperature. The offset current is therefore negligible.

ON Resistance

In a bipolar transistor, ON resistances of about 20Ω are obtained. The ON resistance of the m-o-s transistor is a function of the channel resistivity and may be derived from the equation:

$$I_D = \beta[V_{DS}(V_G - V_{DS}) + (V_{DS}^2/2)] \qquad \ldots(1)$$

where $\beta = g_m^2/2I_{DS}$ at any value of I_{DS}.

If V_{DS} is small compared with V_G:

$$I_D = \beta V_{DS} V_G \text{ or } V_{DS}/I_D = 1/\beta V_G. \qquad \ldots(2)$$

V_G is in fact $V_{GS} - V_{(P)GS}$. Therefore

$$r_{on} = \frac{1}{\beta(V_{GS} - V_{(P)GS})}. \qquad \ldots(3)$$

With the parameters of the BSX82 this gives $r_{on} < 1\text{k}\Omega$ at $V_{GS} = +5\text{V}$. Fig. 3 gives a typical curve of resistance against gate-to-source voltage. This is the only parameter of the bipolar which is superior to the m-o-s transistor. Its importance in the shunt chopper is that in the ON state the unwanted output is $V_{in}[r_{on}/(r_{on} + R_S)]$ where R_S is the effective source resistance (Fig. 4). If this output is not small compared with unity the gain is decreased, and as the resistance tends to be temperature dependent the gain, which is the difference between the outputs in the two states, will also be temperature dependent. This may, however, be overcome with negative feedback, and the comparatively high resistance is not a serious disadvantage.

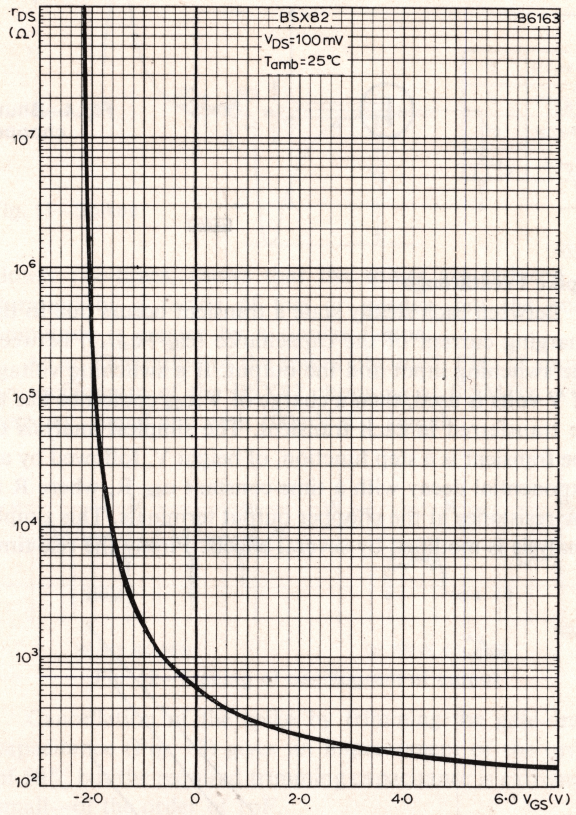


Fig. 3—Variation of r_{DS} with gate voltage

OFF Resistance

When a bipolar transistor is used the maximum source resistance is normally determined by the offset current of the chopper. For example, an offset current of 1μA produces 100mV error in a source resistance of 100kΩ. The OFF resistance is therefore unimportant provided that it is much greater than 100kΩ. As the offset current is negligible in an m-o-s transistor, the source resistance is limited only by the need to supply a discharge path for the spike feedthrough. At low chopping frequencies, source resistances of the order of a few megohms are possible, and the OFF resistance becomes important. The value of the OFF resistance is the slope of the curve I_{DS} against V_{DS}, and is of the order of 100MΩ when $V_{GS} = -5\text{V}$. With signals above a few millivolts the error current tends toward I_{DSX}.

SIMPLE CHOPPER

Offset Voltage and Current

Measurements made on a simple chopper circuit (Fig. 4) confirm that the offset voltage is very small, of the order of 8μV. This will be higher unless great care is taken to shield the circuit from air currents. The temperature coefficient of offset, with similar precautions, can be kept down to 0·2μV/degC. Fig. 5 shows typical results of measurements to determine the temperature coefficient of offset. This is an overall measurement with no attempt to separate the voltage, current, and spike contributions.

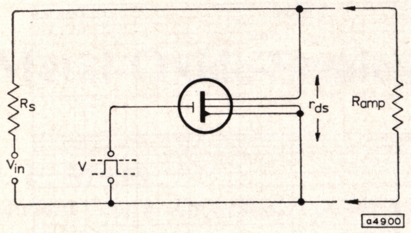


Fig. 4—Shunt chopper

Spike Feedthrough

Between each steady state a transient occurs due to the charging current of the capacitance ($c_{dg}+c_{stray}$) between the switching input and the output. If a switching voltage of V volts is used, then a charge of $V.c_{dg}$ coulombs has to be transferred in each transient. The simplest analysis of the transient is a step function, of height V, followed by an exponential decay with a time-constant $c_{dg}.R$, where R is the resistance at the chopper output terminals. This simple analysis is modified by several effects. Firstly the rise-time is finite, being affected by the mode of generation of the square wave and by the gate capacitances. Secondly, the peak voltage is much less than V_S as the charging current of the capacitor c_{dg} is instantaneously partly absorbed by the capacitor c_{ds} and the circuit stray capacitance (Fig. 6). Thirdly, the resistance into which the charging current flows to give the exponential decay is partly determined by the resistance of the device, which is itself dependent on the rapidly varying gate-to-source voltage. The time-constant of the exponential decay is, therefore, time-variable. Fourthly, the transient is modified by the bandwidth of the amplifier. In the extreme, if the amplifier saturates, the spike is extended in time as the hole storage charge of the saturated transistor holds the transistor on after the transient should have ended.

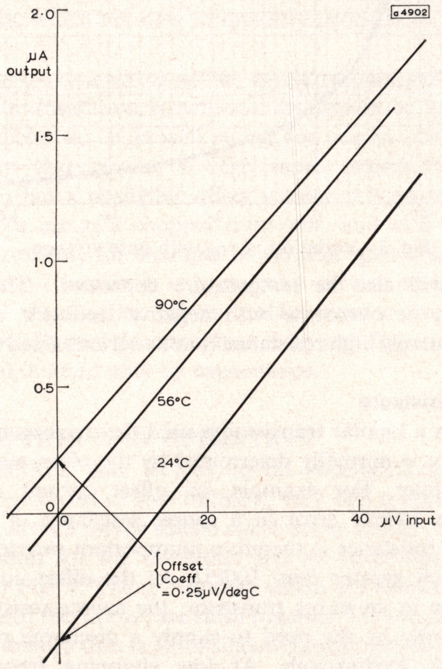


Fig. 5—Offset×temperature

From these considerations it is evident that an exact calculation of the spikes would be extremely difficult. An approximation which gives adequate results is merely to quote the spikes as a charge, in pico-coulombs. To convert this into a voltage error a typical calculation would proceed as follows:

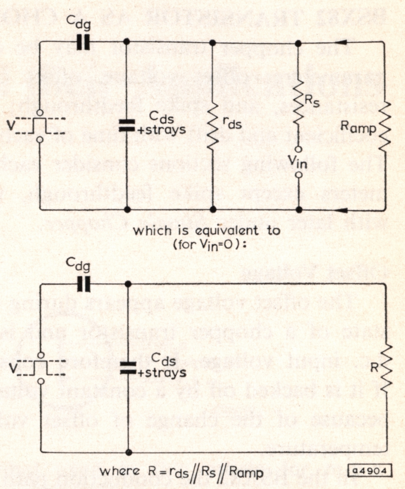


Fig. 6—Spike-forming circuit

Take the spike charge as $10V \times 0{\cdot}5pF = 5pC$. As $CV = \int I.dt$, or $CV = I_M t$ where I_M is the mean current, the spike could be 5μA for 1μs or 0·5μA for 10μs etc., depending on the discharge path. The effect of the spike is, however, independent of the time distribution of the charge and may be averaged over half the switching cycle provided that this time is longer than the spike duration.

For example, switching at 5kHz gives 0·1ms half period and $I_M = 5pC/0{\cdot}1ms = 50nA$. With 10kΩ load this is equivalent to an error of $50nA \times 10k\Omega = 500\mu V$. This may be backed off, as the temperature coefficient of the spike area is low.

Performance

The equivalent circuit of the spike-forming network is shown in Fig. 6. From this the expected transient would be of height $V.c_{dg}/(c_{dg}+c_{ds})$ and the decay time-constant $R(c_{dg}+c_{ds})$. Taking c_{dg} as 0·7pF and c_{ds} as 5pF together with a further 3pF for stray capacitances, transient height $= 10V \times 0{\cdot}7/8{\cdot}7 = 810mV$. Taking the source resistance (Fig. 4) as 15kΩ and the amplifier input resistance as 40kΩ, transient time-constant $= 8{\cdot}7pF \times 15 \times 40k\Omega/55 = 0{\cdot}08\mu s$.

The principal deviation from these theoretical values is caused by the rise-time of the switching waveform. As an exponential fall to 10% takes 2·3×CR, the theoretical values would be 810mV and 0·18μs. Spikes were measured on several transistors, taking the maximum height, and duration at the 10% points. Typical results are 150mV and 1μs, as in Fig. 7, which shows the effect of finite rise-time in extending and flattening the transient. The area of the spike agrees well with the theory as $810mV \times 0{\cdot}18\mu s = 146 \times 10^{-9}V\,s$, and $150mV \times 1\mu s = 150 \times 10^{-9}V\,s$.

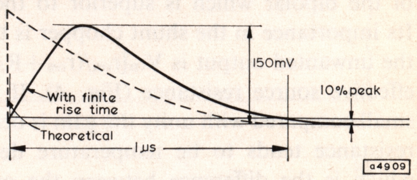


Fig. 7—Spike (shunt chopper)

SPIKE CANCELLATION BY THE SERIES-SHUNT CONFIGURATION

The form of the spike in the shunt chopper was examined in *Spike Feedthrough* (page 56). It was found to consist of a voltage rise-time-constant determined by the switching signal rise-time and modified by the c_{gs} of the device, followed by an exponential decay. The decay-time-constant is determined by c_{dg} in parallel with c_{ds} and the stray capacitances, and a resistance R, which is the input resistance of the amplifier R_{amp} in parallel with the source resistance, R_S, and the device resistance r which varies with time over the spike period. The current × time integral of the resulting spike is $V_S.c_{dg}$.

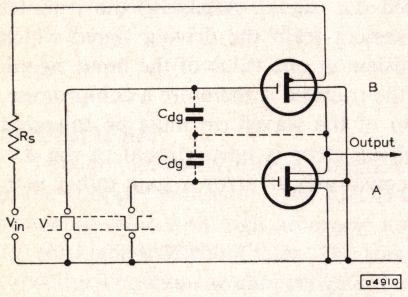


Fig. 8—Series-shunt chopper

In the series-shunt configuration (Fig. 8) a charge is inserted from each switching waveform, and as the waveforms are in antiphase the two charge insertions are of opposite polarity and tend to cancel. If the inputs are derived from the same circuit, such as a bistable or phase-splitter, the rise-times are likely to be similar, and the resistive discharge path is common to the two transistors. The only parameter which affects the cancellation is therefore the c_{dg} of each transistor.

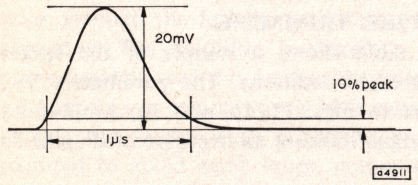


Fig. 9—Spike (s-s chopper)

Fig. 9 shows a typical result. Several pairs of transistors were tried and results between 1mV, 1·2μs ($0{\cdot}8 \times 10^{-9}V\,s$) and 40mV, 1μs ($25 \times 10^{-9}V\,s$) were obtained. Distortion of the rise-times by severely unequal values of c_{gs} gave rise to unequal time distributions of spike in a few cases, and spike shapes were obtained as in Fig. 10. The areas of these spikes were very small (about $10^{-9}V\,s$).

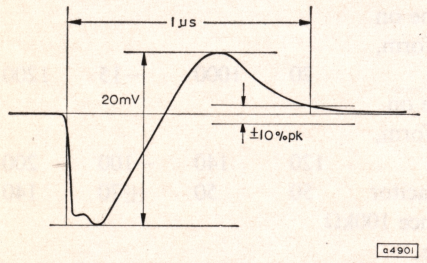
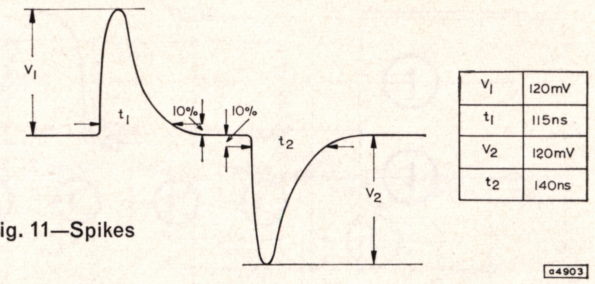


Fig. 10—Distorted spike (s-s chopper)

If a driving waveform with faster rise-time (20ns) is used, then with a series-shunt chopper, and low source resistance (100Ω), spikes are obtained as shown in Fig. 11.

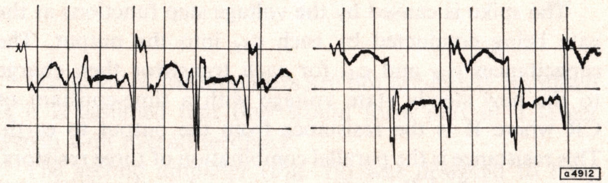
Comparing these results with previous results, using slower rise-times, shows that the spikes are reduced in duration by a factor of five or greater, but the peak amplitude is greater by a similar factor.



V_1	120mV
t_1	115ns
V_2	120mV
t_2	140ns

Fig. 11—Spikes

As an illustration of the spikes obtained, Fig. 12 shows an oscillogram of the BSX82 chopping at 0·5MHz, with zero d.c. signal and with 100mV d.c. signal.



(a) Zero d.c. signal (b) 100mV d.c. signal

Fig. 12—Tracing of oscillogram of output

Cancellation of the spike by trimming the gate-drain capacitance (Fig. 13) gives an improvement of the order of 50% but the required trimming capacitance is extremely small—of the order of 1pF.

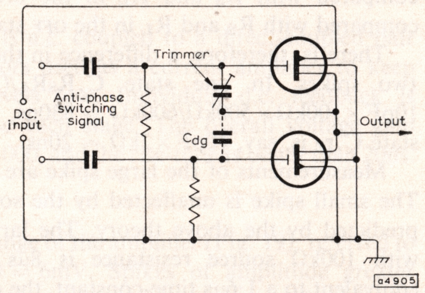


Fig. 13—Trimming capacitor

SPIKE CANCELLATION BY ADJUSTMENT OF OTHER PARAMETERS

When the spike is trimmed by a capacitor, as described above, the method of trimming ensures that the charge inserted by one path is equal to the charge inserted by the other. The variation with time of the charging current is not controlled, and differences in the shapes of the two spikes give an output as shown in Fig. 10. The integrated area of this spike, and therefore the difference of the charge insertions, is zero, but the spike is still large.

Three possible causes of the difference between the two spikes are firstly, the differences of the feedthrough paths, as the capacitors are in practice complex impedances, secondly the differences of the driving waveforms, and thirdly the difference of the transfer characteristics during the transient periods.

The first and third effects are outside the control of the circuit designer. Some control may be exercised over the driving waveform, for example by using a symmetrical phase-splitter to drive the two transistors. It was found that in practice the improvement obtained was not significant.

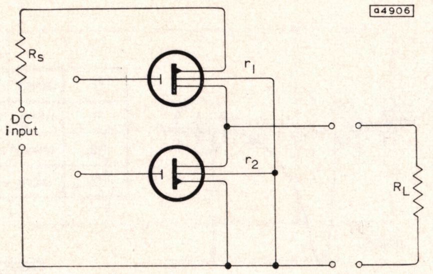


Fig. 14—Series-shunt chopper with source resistance

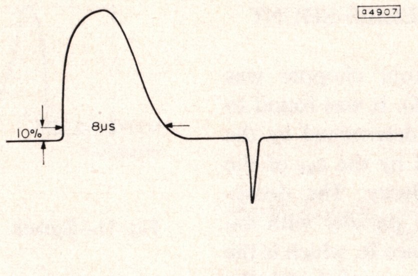


Fig. 15—Spikes with 100kΩ source resistance

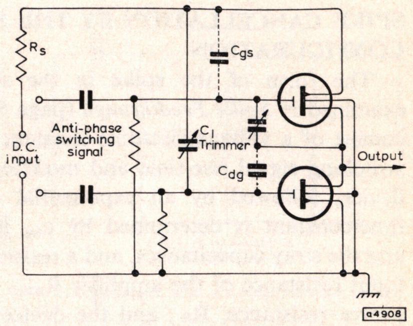


Fig. 16—Trimmer for high source resistance

EFFECT OF SOURCE RESISTANCE ON SPIKES

So far the effect of source resistance (R_s in Fig. 14) has been ignored.

The spike is caused by the voltage step functions at the gate being conducted by each c_{dg} into the output. The capacitances c_{dg} and c_{ds} for each transistor then charge to the new steady state voltage with a time-constant of CR where R is the resistance from the output to earth. This resistance is the parallel combination of three resistors, $R_s + r_1$, r_2, and R_L, where r_1 and r_2 are the resistances of the two transistors and R_L is the resistance of the amplifier.

In one state, when r_1 is high and r_2 is low, R becomes r_2; in the other state r_2 is high and r_1 low and R becomes R_s in parallel with R_L (assuming that r_1 and r_2 are small compared with R_s and R_L in the ON state, and large compared with R_s and R_L in the OFF state).

There is, therefore, a difference in the durations of the two spikes. In one state $C.R_sR_L/(R_s+R_L)$ is, say, $10\text{pF} \times 100\text{k}\Omega \times 500\text{k}\Omega / 600\text{k}\Omega = 830\text{ns}$, and in the other state $C.r_2$ is, say, $10\text{pF} \times 2\text{k}\Omega = 20\text{ns}$.

Measurements of the large spike are shown in Fig. 15. The small spike is unaffected by the source resistance as predicted by the above theory. The large spike duration with 100kΩ source resistance is 8μs for 90% decay, equivalent to a 1·6μs time-constant, the order of the result (830ns) predicted above.

This large spike may be trimmed out by injecting into the source resistance a voltage step in antiphase to the undesired spike. As a series-shunt chopper is being used this antiphase signal is available at the other gate, and may be injected by the capacitor C_1 in Fig. 16. By adjustment of this capacitor the large spike may be trimmed out, leaving the feedthrough spikes as found in the low source resistance case.

When a d.c. signal is introduced the trimming capacitor requires readjustment to give the best square wave, and the capacitance required varies with the d.c. signal. This may be due to the voltage dependence of the device capacitance, or possibly to the variation of device resistance, as follows.

During the changeover time, as one resistance is falling (from r_{off} to r_{on}) and the other rising (from r_{on} to r_{off} in parallel with R_L) the series combination has a resistance which falls from r_{off} to a minimum, then rises to R_L (with the previous approximations). As the chopper forms a potential divider with the source resistance, a transient signal is injected into the output of amplitude proportional to the applied d.c. signal. Adjusting the trimmer inserts a second transient from the driving signal which cancels the first transient at one value of the input signal. The best setting of the trimmer is therefore a compromise, and some distortion of the waveform must be tolerated (Fig. 17). The resulting error is proportional to the d.c. signal. It therefore constitutes an error in gain rather than a zero error.

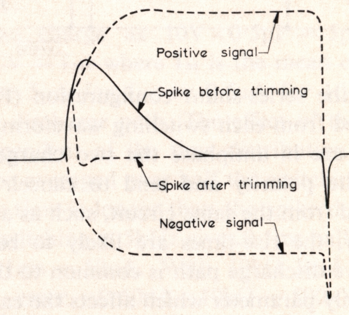


Fig. 17—Distortion by trimmer capacitor

RESULTS OF SPIKE TRIMMING

The following table shows a sample of the spikes obtained under several conditions. The parameters V_1, V_2, t_1 and t_2 refer to Figs. 11, 15, and 10. Amplitudes quoted with both signs indicate an overcorrected spike as in Fig. 10.

TABLE 1

Spike Amplitudes and Durations

Condition	V_1 (mV)	t_1 (ns)	V_2 (mV)	t_2 (ns)
Source resistance ~ 2kΩ				
200ns rise-time on driving waveform, no correction	20	1000	−15	1200
20ns rise-time on driving waveform, no correction	120	140	−100	200
20ns, c_{dg} capacitor	50	50	±70	140
Source resistance 100kΩ				
20ns rise-time, no correction	1000	10 000	−350	150
20ns c_{g2s1} capacitor	150	200	±160	180
20ns c_{g2s1} and c_{d2g2} capacitors	±150	200	±100	160

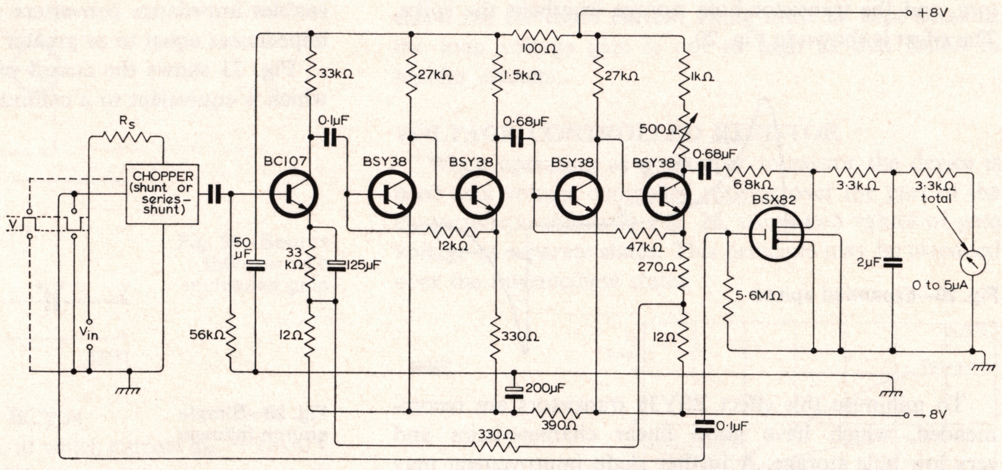


Fig. 18—Chopper amplifier

AMPLIFIERS

Two amplifiers have been designed to use the BSX82 m-o-s chopper transistor. The first (Fig. 18) is for lower switching rates with high accuracy, and the second (Fig. 19) for higher switching rates. The leakage of the coupling capacitor between the chopper and the amplifier (Fig. 18) can cause an error, as the bias voltage on the first base provides a second input signal, being chopped through the capacitor leakage.

In the first amplifier this bias voltage is minimised by using a simple C-R coupling to earth and using positive and negative rails to supply the bias to the first stage. An alternative method, using an m-o-s transistor in the first stage, is employed in the second amplifier circuit. A similar problem exists at the demodulator of each amplifier, which tends to chop the collector voltage of the last stage through the leakage resistance of the demodulator capacitor. The amplifier is therefore designed to have approximately zero d.c. level at the output.

As there is a comparatively high current circuit present, namely the square wave generator, considerable care is required to avoid earth loops, common impedances and pick-up.

The gains of the amplifiers are not accurately stabilised as it is assumed that they would form part of a larger system with overall feedback.

The second amplifier (Fig. 19) was designed to have sufficient frequency response to avoid distortion of a transient with 20ns rise-time.

The first stage is a BFX63 m-o-s transistor, giving a high input impedance without adversely affecting the bandwidth. A high drain current (3mA) is used to keep the drain resistor low, and to increase the mutual conductance.

The first stage is a.c. coupled to a direct-coupled pair of BSY38 transistors used as a current amplifier to keep the impedance levels low. Individual d.c. feedback is applied to stabilise each stage. The overall voltage gain of the amplifier is 1000, and the rise-time is better than 20ns.

Saturation Effects

The dynamic range of the amplifier (Fig. 19), referred to input, is 6V/1000 = 6mV. Spikes of amplitude greater than this will bottom one or more of the amplifier transis-

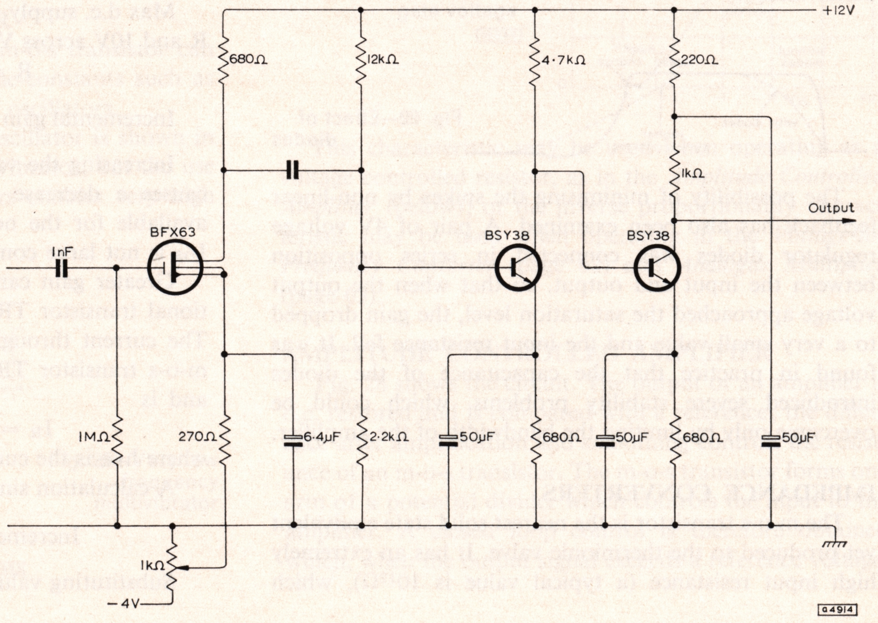


Fig. 19—High-frequency chopper amplifier, with BSX82 chopper input, similar to that shown in Fig. 18

tors, and the transistor hole storage lengthens the spike. The effect is shown in Fig. 20.

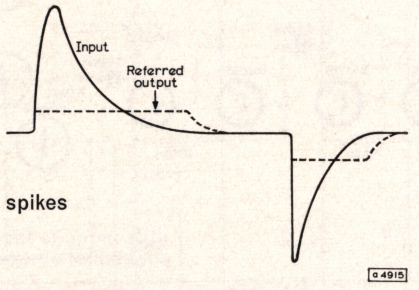


Fig. 20—Expanded spikes

To minimise this effect BSY38 transistors are recommended, which have good linear characteristics and very low hole storage. A further slight improvement may be obtained by connecting diodes from base to collector of each stage (Fig. 21). Providing that the diode forward voltage is less than the V_{bc} of the bottomed transistor, (that is, $V_f < V_{be} - V_{ce(sat)}$) then the diode prevents saturation of the transistor and only the hole storage of the diode extends the spike. A germanium diode must be used to satisfy the above condition, and the AAZ13 is recommended as its hole storage is only 30pC. It is found, however, that as the diode is connected from collector to base, its capacitance is amplified by Miller effect, and the bandwidth is affected. Fig. 22 shows a typical result. The slight improvement in hole storage is therefore offset by the spreading of the spike through loss of bandwidth.

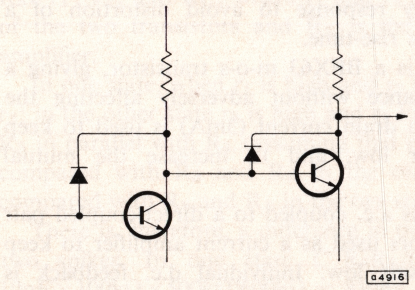


Fig. 21—Diodes in amplifier

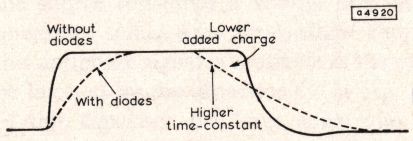


Fig. 22—Effect of diodes

The possibility of minimising the spikes by non-linear feedback has also been examined. A pair of 4V voltage regulator diodes was connected in series opposition between the input and output, so that when the output voltage approached the saturation level, the gain dropped to a very small value and the input resistance fell. It was found in practice that the capacitance of the diodes introduced severe stability problems, which could be overcome only by limiting the bandwidth of the amplifier.

IMPEDANCE CONVERTERS

The m-o-s transistor is the nearest solid state equivalent yet produced to the thermionic valve. It has an extremely high input resistance (a typical value is $10^{12}\Omega$), which enables impedance converters to be designed with input impedances equal to or greater than that of valve circuits.

Fig. 23 shows the circuit of a simple source follower which is equivalent to a cathode follower.

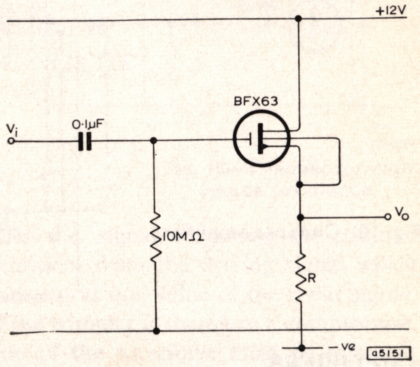


Fig. 23—Simple source follower

Because of the resistance R, the true input to the transistor is $V_i - I_{DS}R$, part of which is used to overcome the pinch-off voltage $V_{(P)GS}$. Therefore, the effective input is $V_i - I_{DS}R - V_{(P)GS}$.

$$\text{Output} = I_{DS}R. \qquad \ldots(4)$$

$$I_{DS} = g_m(V_i - I_{DS}R - V_{(P)GS}). \qquad \ldots(5)$$

$$\frac{I_{DS}}{g_m} = V_i - I_{DS}R - V_{(P)GS}. \qquad \ldots(6)$$

$$I_{DS}[(1/g_m) + R] = V_i - V_{(P)GS}. \qquad \ldots(7)$$

$$\text{Output} = I_{DS}R = (V_i - V_{(P)GS}).\frac{R}{(1/g_m)+R}$$

$$= (V_i - V_{(P)GS}).\frac{g_mR}{1+(g_mR)}. \qquad \ldots(8)$$

$$\text{Incremental gain} = \frac{d(I_{DS}R)}{dV_i} = \frac{g_mR}{1+(g_mR)}. \qquad \ldots(9)$$

Substituting values for the BFX63,

$g_m = 2{\cdot}5\text{mA/V}$ typical at $I_{DS} = 5\text{mA}$.

As $g_m \propto \sqrt{I_{DS}}$

$g_m = 1{\cdot}1\text{mA/V}$ typical at $I_{DS} = 1\text{mA}$.

Max d.c. supply = 20V, therefore, allowing 10V across R and 10V across V_{DS},

$$R = 10\text{V}/1\text{mA} = 10\text{k}\Omega.$$

$$\text{Incremental gain} = \frac{g_mR}{1+(g_mR)} = \frac{1{\cdot}1\times10}{1+(1{\cdot}1\times10)} = 0{\cdot}92.$$

Increasing the value of R increases the gain, but also causes a decrease in current, therefore less current is available for the next stage. The limit is reached when I_{DS} is not large compared with the cut-off current, I_{DSX}.

Greater gain can be obtained by including a conventional transistor TR_2 in the circuit as shown in Fig. 24. The current through R is now the drain current of the m-o-s transistor TR_1, plus the collector current of TR_2 and is

$$I_R = g_m(V_{GS} - V_{(P)GS})h_{FE} \qquad \ldots(10)$$

where h_{FE} is the current gain of TR_2.

A calculation similar to the above gives

$$\text{Incremental gain} = \frac{h_{FE}g_mR}{1+(h_{FE}g_mR)}. \qquad \ldots(11)$$

Substituting values for the BFX63 and BCY34:

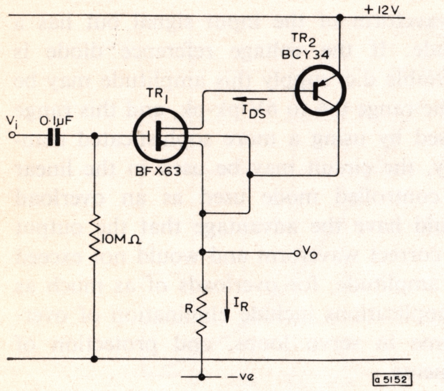


Fig. 24—Source follower with increased gain

If we take 20mA in the BCY34

$I_{DS} = 20/30 = 0{\cdot}66\text{mA}$, at which current $g_m = 1\text{mA/V}$

$$R = \frac{10\text{V}}{20\text{mA}} = 500\Omega$$

$$\text{gain} = \frac{30\times1\times0{\cdot}5}{1+(30\times1\times0{\cdot}5)} = 0{\cdot}94$$

giving a slightly improved gain, with a current availability of 20mA instead of 1mA.

By choice of a suitable resistance the gain could be much increased at a current availability of 1mA.

The output resistance is given by

$$r = \frac{R}{1+(g_mR)} \text{ for Fig. 23} \qquad \ldots(12)$$

and

$$r = \frac{R}{1+(h_{FE}g_mR)} \text{ for Fig. 24.} \qquad \ldots(13)$$

Substituting as before,

$$r = \frac{10}{1+(1{\cdot}1\times10)} = 830\Omega \text{ (Fig. 23)}$$

or

$$r = \frac{0{\cdot}5}{1+(30\times1\times0{\cdot}5)} = 31\Omega \text{ (Fig. 24).}$$

The effect of the additional bipolar transistor is, therefore, to increase the gain and current availability and decrease the output resistance.

LOW FREQUENCY OSCILLATOR

The high input resistance of the m-o-s transistor can be used in circuits requiring high time-constants such as 'sample and hold' circuits and v.l.f. oscillators.

An example of a low frequency oscillator is shown in Fig. 25. This is a conventional multivibrator, but the use of a pair of BFX63 m-o-s transistors enables very high timing resistors to be used. The required gate swing and, therefore, the drain current swing must be kept small as the loop voltage gain is not as high as that found in bipolar circuits.

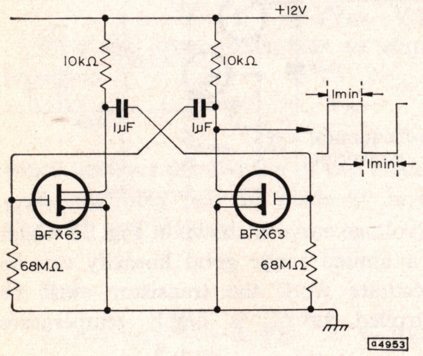


Fig. 25—Very low frequency multivibrator

VOLTAGE CONTROLLED RESISTOR

When operating as a chopper transistor the device is used as a voltage controlled resistor over the part of the characteristic shown in Fig. 26, using two values of gate voltage as separate states. This principle may be extended over the intermediate states.

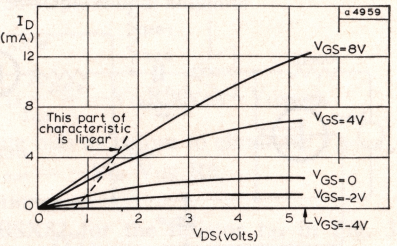


Fig. 26—Output characteristics at low voltages

In this mode the device is characterised by the equation

$$I_D = \beta(V_G V_{DS} - V_{DS}^2/2) + I_{DSX}, \qquad \ldots(14)$$

where

$$V_G = V_{GS} - V_{(P)GS}$$

or if V_{DS} is negligibly small compared with V_G, and neglecting I_{DSX},

$$I_D \simeq \beta V_G V_{DS}.$$

As with these assumptions I_D bears a linear relationship with V_{DS} the device is a pure resistance when viewed between drain and source, and the value of this resistance as shown in Fig. 27, is inversely proportional to the gate voltage:

$$\frac{V_{DS}}{I_D} = r_{ds} = \frac{1}{\beta(V_{GS} - V_{(P)GS})} \qquad \ldots(15)$$

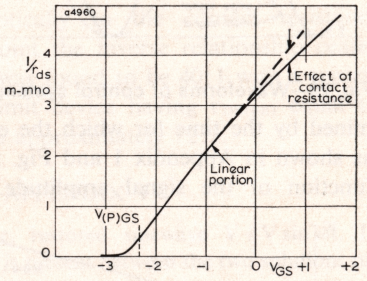


Fig. 27—Drain-to-source resistance against gate voltage

This characteristic may be used when operating as a voltage controlled resistor, as in the *Amplitude Controlled Amplifier* (below); or the inverse proportionality characteristic may be used when operating in the *Voltage-to-Frequency Converter* (page 62) and *Analogue Multiplier* (page 63).

AMPLITUDE CONTROLLED AMPLIFIER

Fig. 28 shows the circuit. The output of an amplifier is d.c. restored and is compared with a reference; the difference after amplification and smoothing controls the resistance of an m-o-s transistor. The m-o-s transistor forms one arm of a potential divider which controls the input to the amplifier. A closed loop control is therefore obtained which, when the output signal exceeds a reference voltage, lowers the gain of the system and stabilises the output voltage.

To obtain the maximum control range the m-o-s transistor should have a resistance large compared with 100kΩ with zero V_{GS}. As the BSX82 is a depletion type, it should be biased to the high resistance region by connecting the gate via the 470kΩ collector load of the BFX12 to a negative voltage of amplitude greater than $V_{(P)GS}$. When the peak of the d.c. restored signal exceeds the regulator diode reference voltage the transistor conducts. As the transistor stage voltage gain is very high (×1000) a very small error signal (10mV) saturates the transistor, giving a square wave output which is smoothed to provide the d.c. signal to the m-o-s transistor. The mark-space ratio of the square wave is determined by the time for which the error signal is present, as shown in Appendix 1 and Fig. 29. This is an inverse function of the signal amplitude. The stabilisation is therefore greatest for errors slightly greater than the level at which stabilisation begins, and deteriorates as the error increases. Fig. 30 shows this effect. This circuit is useful in two ways. Firstly, when used in the controlled mode it provides a signal which is a reproduction of the frequency and waveform of the input signal but has a constant amplitude. If the voltage reference diode is replaced by a variable d.c. supply this amplitude may be controlled over the range 0·6 to 6V pk-pk, and this range would be increased by using a more sophisticated comparator. Secondly, the circuit may be used in the linear mode, and the controlled mode used as an overload limiter. This would have the advantage that the output would be of the correct waveform and would not exceed a predetermined amplitude, for overloads of as much as 200:1. Possible applications include elimination of overload recovery time in servo loops, and protection of recording instruments.

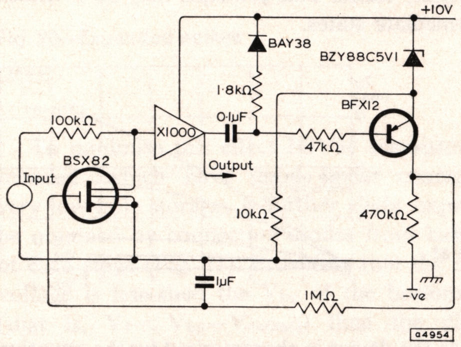
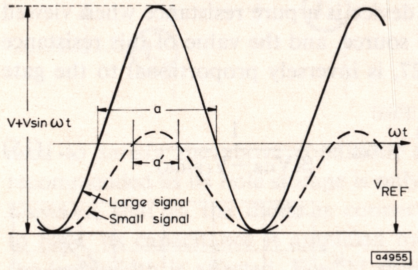


Fig. 28—Amplitude controlled amplifier



a and a′ are the durations of the error signal

Fig. 29—Waveforms of control system

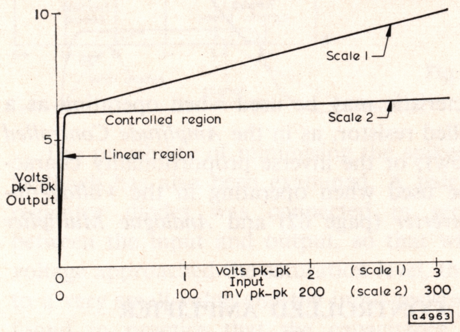


Fig. 30—Transfer characteristic of amplitude controlled amplifier

VOLTAGE-TO-FREQUENCY CONVERTER

The drain-source resistance of the m-o-s transistor has been shown to be inversely proportional to the gate voltage. If the m-o-s transistor is used as the resistive element in a C–R oscillator whose frequency is inversely proportional to resistance, then the frequency will be a direct function of voltage:

$$\text{As } r_{ds} = \frac{1}{\beta V_G} \text{ and } f = \frac{1}{KCr_{ds}}$$

$$\text{then } f = \frac{\beta V_G}{KC} \text{ where K is constant.} \qquad \ldots(16)$$

The oscillator selected was the p-n-p/n-p-n relaxation oscillator in Fig. 31. Substituting an m-o-s transistor for the frequency controlling resistor gives the circuit of Fig. 32. The output is not linear for two reasons; firstly as the signal is not small compared with the gate voltage the drain current of the m-o-s transistor is no longer linear with gate voltage, and secondly the oscillator frequency is not proportional to 1/(CR), but to 1/(CR+t) where t is the recovery time of the circuit.

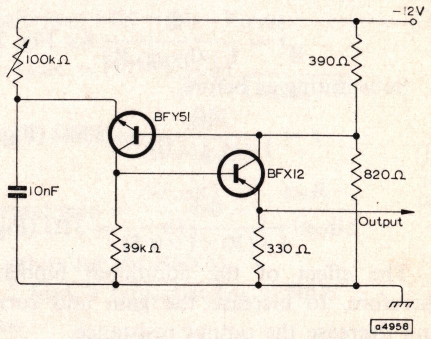


Fig. 31—Basic oscillator

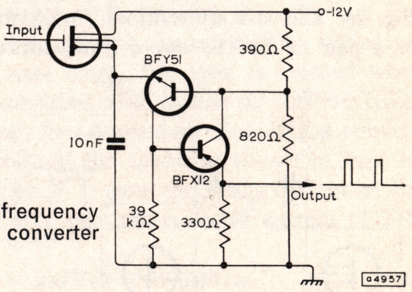


Fig. 32—Voltage-to-frequency converter

The frequency/voltage curve is shown in Fig. 33 which shows that over a limited range good linearity can be obtained. For accurate work the transistor must be temperature controlled as r_{ds} is highly temperature dependent.

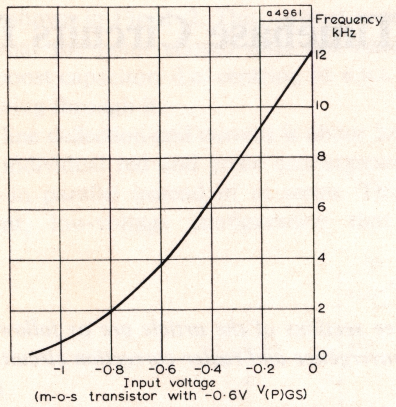


Fig. 33—Voltage-to-frequency converter

The circuit would be useful to convert an analogue voltage to an analogue frequency for transmission in a noisy environment, as a frequency-swept oscillator, or as an element in a closed-loop frequency control system.

ANALOGUE MULTIPLIER

In *On Resistance* (page 55) it was shown that if the drain-to-source voltage of an m-o-s transistor is kept small compared with $V_{GS}-V_{(P)GS}$, then the resistance between drain and source is (Eq. 3)

$$r_{ds} = \frac{1}{\beta(V_{GS}-V_{(P)GS})}.$$

If this resistance is used as one branch of a potential divider (Fig. 34) the output of the potential divider becomes:

$$V_{in}\frac{r_{ds}}{R+r_{ds}},$$

where R is the other arm of the divider.

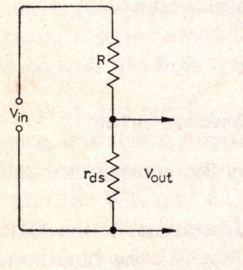


Fig. 34—Potential divider

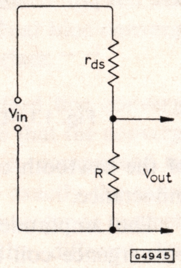


Fig. 35—Inverted form

If $R \gg r_{ds}$, then $V_{out} \simeq V_{in}\frac{r_{ds}}{R}$ which is:

$$V_{out} \simeq V_{in}\frac{1}{R\beta.(V_{GS}-V_{(P)GS})}.$$

With the appropriate bias to eliminate $V_{(P)GS}$ this becomes:

$$V_{out} \simeq \frac{V_{in}}{R\beta V_{GS}},$$

which achieves the division of two analogue quantities.

A multiplier may be made by inverting the divider (Fig. 35) and making

$$r_{ds} \gg R,$$

so that

$$V_{out} = V_{in}\frac{R}{R+r_{ds}} \simeq V_{in}\frac{R}{r_{ds}} = V_{in}R\beta(V_{GS}-V_{(P)GS}).$$

A multiplier was found to have a range of about 4:1 with an accuracy of ±1% for input voltages of between 100mV and 500mV with R = 10kΩ.

The approximation $R \gg r_{ds}$, or $r_{ds} \gg R$ can be eliminated by the use of an operational amplifier (Fig. 36).

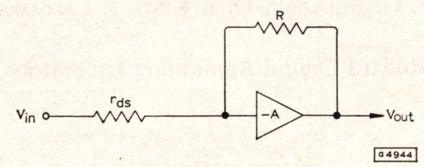


Fig. 36—Operational amplifier

Then:

$$V_{out} = -V_{in}\frac{R}{r_{ds}} = -V_{in}R\beta(V_{GS}-V_{(P)GS}).$$

Adjusting the gate bias as before to eliminate $V_{(P)GS}$,

$$V_{out} = -V_{in}\ V_{GS}.R\beta,$$

an exact multiplication.

Substituting a BSX82 for the resistor r_{ds} in Fig. 36 gives the circuit of Fig. 37. This was measured with a d.c. input signal of 1mV and R = 100kΩ. The limits of the linear range were found to be (a) at the low gain extreme where the gate voltage exceeded the pinch-off voltage and (b) at the high gain extreme where the resistance of the device falls asymptotically to the contact resistance (Fig. 27). At each point the inverse relationship ceases to apply. This range was found to be 40:1 with a typical device; but with a limit device having $r_{DS(on)}$ equal to 1kΩ this would fall to approximately 12:1.

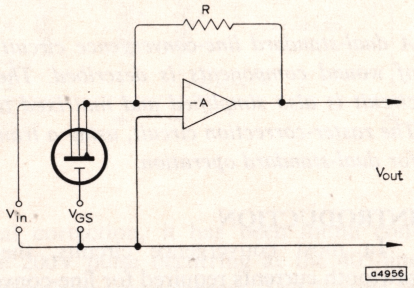


Fig. 37—M-O-S transistor in operational amplifier

APPENDIX 1

The signal is a d.c. restored sinewave V+V sin ωt. In Fig. 29, the error signal is present between the two solutions of:

$$V+V\sin\omega t = V_{REF}$$

hence

$$\omega t_1 = \sin^{-1}\left(\frac{V_{REF}-V}{V}\right) = \sin^{-1}\left(\frac{V_{REF}}{V}-1\right)$$

and

$$\omega t_2 = \pi-\sin^{-1}\left(\frac{V_{REF}}{V}-1\right).$$

The duration is therefore

$$a = \pi-2\sin^{-1}\left(\frac{V_{REF}}{V}-1\right).$$

The gain of the circuit is a function of

$$\frac{da}{dV} = -2\frac{1}{\sqrt{1-\left(\frac{V_{REF}}{V}-1\right)^2}}\times V_{REF}\left(-\frac{1}{V^2}\right)$$

(change of output for change of input)
from which

$$\frac{da}{dV} = \frac{2}{V}\sqrt{\frac{V_{REF}}{2V-V_{REF}}}$$

which decreases as V increases.

Convergence, Raster-correction, and Timebase Circuits for 25in Colour Tube

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This article, in three parts, describes convergence, raster-correction, line and field timebase circuits for the Mullard 25-inch 90-degree colour picture tube A63–11X.

The circuits have received full laboratory testing, but must be considered preliminary. Modifications will arise as the work progresses to the final receiver design.

The three sections of the article are as follows:

Part 1: Convergence and raster-correction circuits. *D. J. King*

Part 2: Field timebase *P. G. Boulton*

Part 3: Shunt-stabilised line timebase *J. Lammers and D. Skelton*

Part 1: Convergence and Raster-correction Circuits

A dual-standard line-convergence circuit using a minimum of wound components is described. The field-convergence circuit is also simplified and matrixed to ease adjustment. The raster-correction circuit, using a transductor, is suitable for dual-standard operation.

INTRODUCTION

In most convergence circuits, the paraboloid and sawtooth currents required for line-convergence correction are obtained by integrating a flyback pulse taken from the line output transformer (Ref. 1). Since the integration is large, the control circuits use a considerable number of adjustable wound inductors, the number of which is increased still further by the requirement for 625- and 405-line operation. If a waveform requiring less integration to supply the convergence coils is used, however, a reduction in the number of wound components can be effected.

In this article a circuit is described in which the line-deflection current is used as a convergence waveform source. The setting-up procedure is given on p. 67.

LINE CONVERGENCE

The shape of the current flowing in the line deflection coils is inherently suitable for dynamic convergence, requiring only a small amount of additional integration. Furthermore, it has a stable amplitude; less modification of the waveform by the shaping circuits is required and hence far more consistent convergence is obtained. This is particularly so in the case of a line timebase operated without a constant e.h.t. load.

In the skeleton circuit (Fig. 1.1), the red, green, and blue convergence coils, R, G, and B are connected in series. The complete network is then connected in series with the line deflection coils. Connected in parallel with the red and green convergence coils is a variable resistor RV_B to adjust the amplitude of the convergence current. No further modification of the red and green convergence waveform is normally required since sufficient integration of the sawtooth current is given by the convergence coil inductance.

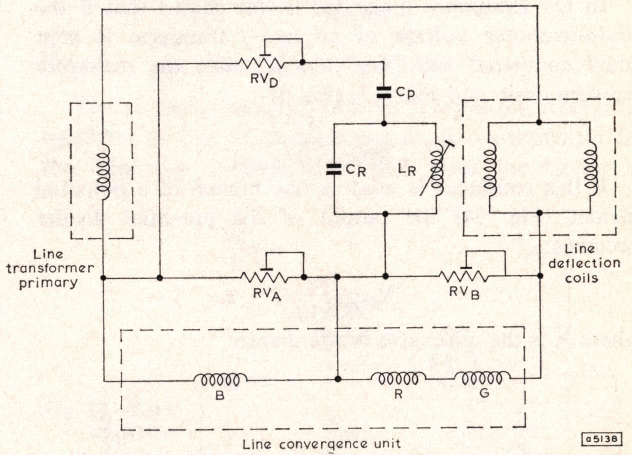

Fig. 1.1—Line-convergence skeleton circuit

The amplitude of the sawtooth current in the blue convergence coil is adjusted by RV_A. As the blue convergence correction requires a predominantly parabolic current, additional integration is required, and is provided by C_p. The waveform produced by this method of integration is basically sinusoidal, however, and requires further modification. This modification is obtained by adding a second-harmonic sinusoidal waveform from the resonant circuit L_R, C_R. The resulting parabolic current is then varied by resistor RV_D.

Fig. 1.2 shows the complete dual-standard line-convergence circuit with its connection to the line output transformer and part of the output circuit. It is normal practice to balance the deflection coils about an 'earthy' point to reduce electrostatic radiation. As it is undesirable to have the convergence coils pulsed several volts above chassis potential, it is preferable to connect the convergence coils into the 'cold' point (that is, the centre point) of the deflection-coil winding on the line output transformer, as shown in Fig. 1.2. This method is satisfactory provided that the point chosen does not have currents from the boost capacitor, d.c. centring or e.h.t. overwind tuning flowing through it.

As the line deflection-coil current is about 3A peak-to-peak, the individual red and green convergence coils are connected in parallel instead of in series. This forms a high-current, low-voltage configuration that is more compatible for connecting into the line-deflection circuit and reduces the dissipation in the control potentiometers. The extra amount of line linearity correction required is also reduced by this parallel connection, and is within the range of adjustment obtainable from the Mullard linearity control, type AT4042/02. As the current required for blue convergence is three times greater than that for red and green, a series connection of the individual blue convergence coils has been found more appropriate.

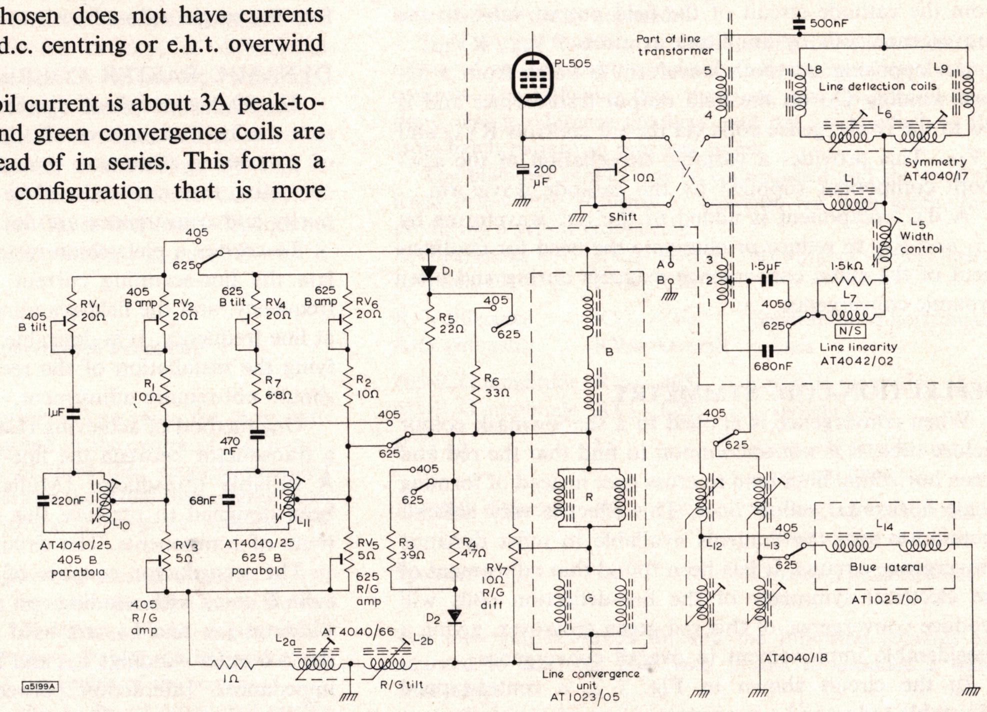

Fig. 1.2—Complete line-convergence circuit

With the requirement for dual-standard line convergence, it is almost impossible to guarantee that the convergence waveforms and, therefore, the d.c. component on both the 405- and 625-line systems are exactly the same. This, in effect, means that the static convergence magnets would require adjustment between the different line standards. As this is impracticable, the circuit shows clamping diodes D_1, D_2. Diode connected (base-emitter strapped) AC128 transistors have a suitable low impedance for this application. The values of the limiting resistors R_3 to R_6 in series with these diodes are chosen not only to ensure exact static convergence on both line standards but to minimise the need for readjustment of the static convergence magnets during and after the dynamic convergence procedure. The resistor values are determined as follows:

The line convergence circuit is short-circuited (point A to point B in Fig. 1.2) and the static magnets are adjusted for centre convergence. The short-circuit between points A and B is removed and the resistor values are chosen so that there is no centre convergence shift when the amplitude controls are varied about the correct dynamic convergence setting on both line standards.

For blue lateral correction, it has been found convenient to use the 200V pulse occurring at the 405-line tapping point on the output transformer. This is used to supply current to the series-connected coils on the blue lateral convergence assembly and is controlled by the appropriate Mullard amplitude coil, type AT4040/18. Alternatively, if parallel-connected blue lateral coils are used, a lower-amplitude pulse, typically 100V, is required with a Mullard control coil, type AT4040/11.

Tilt correction of the R/G waveform, if required, is provided by L_{2a}—L_{2b}. The two small coils are on a single former with an adjustable core. An increase in the inductance L_{2a} differentiates the sawtooth waveform; an increase in L_{2b} gives additional integration of convergence coil current.

Potentiometers RV_1 to RV_7 in the line-convergence circuit, Fig. 1.2, are wire-wound and are used as rheostats. To minimise power dissipation, series limiting resistors are included where appropriate. It is envisaged that suitable potentiometers could be developed for this application, in which the rotation of the wiper is limited so that the series resistance is an inherent part of the potentiometer. The potentiometers in the blue circuit have a 4W rating; the potentiometers in the red/green circuit have a 2W rating.

FIELD DYNAMIC CONVERGENCE

Most field convergence circuits cause degeneration in the timebase. Such effects can be minimised by connecting the convergence coils in parallel in a lower-impedance circuit configuration. Fig. 1.3 shows a circuit for use with this configuration, in which the red and green controls are matrixed for ease of adjustment.

A combined sawtooth-parabola waveform is supplied from the cathode circuit of the field output valve to the convergence coils by amplitude controls RV_{14}, RV_{15}.

An opposing sawtooth waveform is taken from a 32-turn winding L_{27} on the field output transformer and is fed to the convergence coils via the tilt controls RV_{13} and RV_{16}. This provides a variable cancellation of the sawtooth component supplied by the cathode waveform.

A d.c. component is added to the a.c. waveforms by R_{11} and R_{12} to reduce or eliminate the need for readjustment of the static convergence magnets during and after dynamic convergence.

DEFLECTION-COIL SYMMETRY

When convergence is applied to a shadowmask colour picture tube, it is not uncommon to find that the red and green horizontal lines tend to cross over instead of forming single horizontal yellow lines. This effect is very difficult to remove with the controls available in most dynamic convergence circuits. It has been found that adjustment of the electrical symmetry of the line-deflection coils will produce convergence of this red-green crossover, giving a considerable improvement in overall convergence.

In the circuit shown in Fig. 1.2, a centre-tapped adjustable inductor L_6 is connected in series with the two halves of the line-deflection coils. This allows the current flowing in either half of the line coils to be altered, and provides a convenient method of symmetry adjustment.

By incorporating a potentiometer RV_{18} (Fig. 1.3) in series with the two halves of the field-deflection coils, a field symmetry adjustment can also be provided. This adjustment, when used in conjunction with the field-convergence Red/Green difference control RV_{17} (Fig. 1.3), can simplify the convergence of the top and bottom red and green horizontal lines, which would otherwise tend to run parallel to—but separate from—each other, instead of forming single yellow lines.

DYNAMIC RASTER CORRECTION

The 90-degree deflection coils are designed for optimum spot quality and, as a result, it is inevitable that a degree of pincushion distortion remains. This requires external correction that must take place at the deflection centre if purity and convergence are not to be disturbed.

To correct a pincushion raster it is necessary to modulate the line-scanning current with a parabola at field frequency, and the field-scanning current with a parabola at line frequency. It is desirable, in the interests of simplifying the installation of the receiver, that this correction should not require adjustment.

One method of achieving raster correction is to employ a transductor between the line- and field-deflection coils. A suitable transductor (Mullard type AT4041/03) has been designed to produce this correction with the minimum of components. The circuit is shown in Fig. 1.3.

The transductor consists of specially shaped Ferroxcube E cores with windings on all three limbs. The centre windings L_{21} and L_{22} are used for control purposes, and the two outer windings L_{23} and L_{24} are the controlled load impedances. Interaction between the control and load windings is minimised by connecting L_{23} and L_{24} in series opposition. The control winding is connected in series with the field-deflection coils so that the impedance of L_{23} and L_{24} is varied proportionally to the field-scanning current. The load windings are connected across the line-deflection coils and introduce a varying shunt load which modulates the line scan at the field rate. The shaping of the transductor core and its magnetic properties cause this modulation to be approximately parabolic in form, which will counteract the pincushion distortion in the line (east-west) direction.

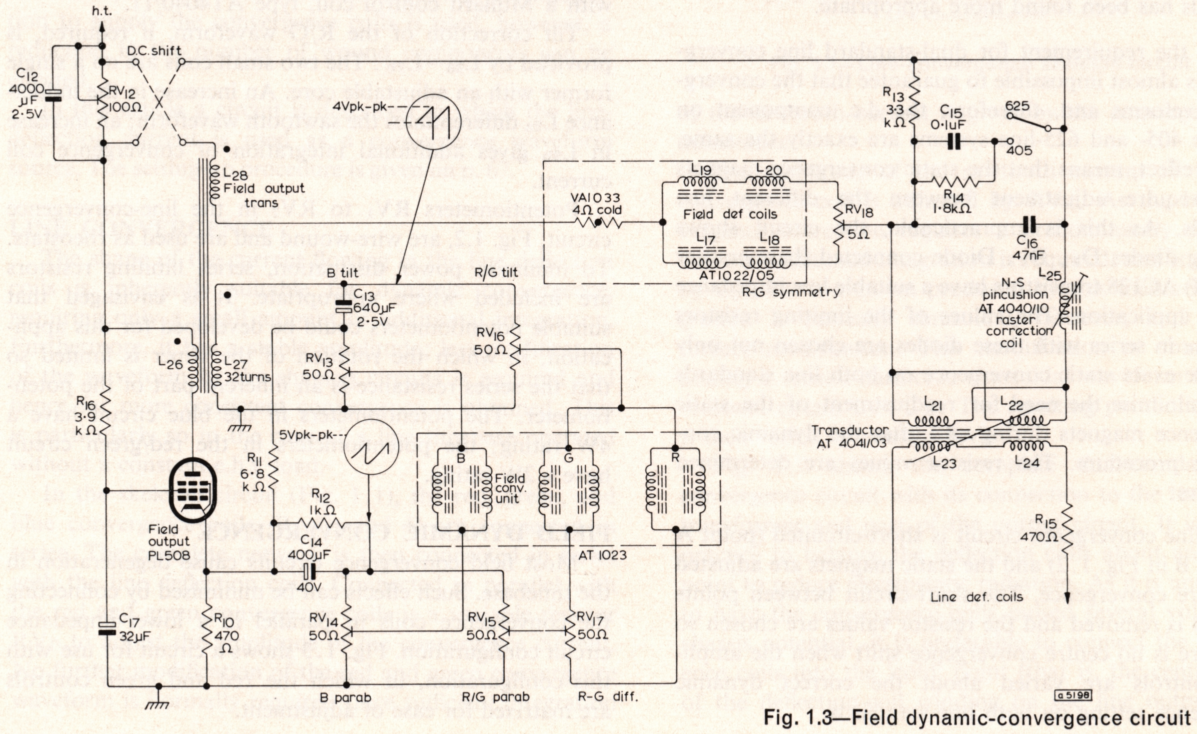

Fig. 1.3—Field dynamic-convergence circuit

North-south correction is obtained by the action of C_{16} integrating the out-of-balance line pulses which are induced in the control winding because of differential saturation of the transductor core by the two load windings. The integrated parabolic voltage across C_{16} introduces a parabolic modulating current in the field-deflection coils. The amplitude of this current is controlled by L_{25} to provide some adjustment of the north-south correction. Since the integrating value of C_{16} is frequency-dependent, an additional capacitor C_{15} is switched in parallel with it for 405-line operation.

APPENDIX: Convergence Procedure

STATIC CONVERGENCE

The object of static convergence is to cause the three individual beams to be superimposed in the centre of the screen. This is achieved by the use of three disc magnets mounted symmetrically 120 degrees apart on the radial convergence yoke with their fields directed into the convergence pole-piece of each electron gun.

As the red and green magnets are located at angles of 120 and 240 degrees respectively they will therefore move the red and green beams along the 120-degree and 240-degree radial axes. Adjustment of these magnets enables the red and green beams to be superimposed at the centre of the screen.

To enable the blue beam also to be superimposed at this point, both horizontal and vertical movement of this beam will be required. The blue radial static magnet is positioned vertically above the blue pole piece, and rotation of it causes the blue beam to move up and down along a vertical axis. The horizontal movement is accomplished by means of a blue lateral convergence magnet which directs the field, from two rod magnets mounted near the base of the picture tube, into the blue gun. Adjustment of both the blue radial and lateral magnets until the blue beam coincides with the converged red and green beams allows static convergence to be completed.

DYNAMIC CONVERGENCE

Convergence of the three beams at the centre of the screen having been achieved, it is necessary to correct for the misconvergence caused by field and line deflection. Before dynamic convergence is begun, it is essential that the receiver should have been degaussed, and the width, line linearity, height, field linearity, and purity adjusted.

It is normal practice to use a white cross-hatch pattern displayed on the screen to assist the adjustment of the dynamic controls. The following lists, therefore, give the control functions, circuit reference numbers, and the visual effect on the cross-hatch pattern in practical terms.

The blue gun should first be extinguished and the controls listed below then adjusted to converge red with green, thus producing a yellow cross-hatch.

R/G parabola	RV_{15}	Bottom	'Bowing' of vertical lines
R/G field tilt	RV_{16}	Top	
R/G difference	RV_{17}	Top	Separation of horizontal lines
R/G symmetry	RV_{18}	Overall	
405-R/G amplitude	RV_3	405	Left side separation of vertical lines
625-R/G amplitude	RV_5	625	
R/G tilt	L_2	—	Right side separation of vertical lines
R/G line difference	RV_7	—	'Bowing' of horizontal lines at top and bottom
Symmetry	L_5	—	Crossover of horizontal lines.

The blue gun is turned on and the following controls are adjusted to converge blue with yellow to produce a white cross-hatch.

Blue field tilt	RV_{13}	Bottom	Separation of blue horizontal lines
Blue field parabola	RV_{14}	Top	
405 blue amplitude	RV_2	405	'Drooping' of blue horizontal lines
625 blue amplitude	RV_6	625	
405 blue tilt	RV_1	405	Crossover of blue horizontal lines
625 blue tilt	RV_4	625	
405 blue parabola	L_{10}	405	'Undulation' of blue horizontal lines
625 blue parabola	L_{11}	625	
405 blue lateral	L_{12}	405	Separation of blue vertical lines at left and right sides.
625 blue lateral	L_{13}	625	

REFERENCE

JOHNSON, P. I., 'Convergence Circuit for use with the AX53-14 Picture Tube'. **Mullard Technical Communications,** Vol. 8, No. 71, August 1964, pp. 5 to 14.

Part 2: Field Timebase

The design is given of a valve field timebase suitable for use with the Mullard A63-11X 25-inch 90-degree colour tube operating at an e.h.t. of 25kV. The field output valve type PL508 is used, together with one section of an ECC82 double triode in a self-oscillating circuit. The output transformer is in a 'zero-initial-slope' mode of operation, and the timebase is suitable for an h.t. supply of 265 to 285V.

CIRCUIT DESCRIPTION

The complete field timebase circuit, including the convergence components, is shown in Fig. 2.1. The design is based on the Mullard deflection coils, type AT1022/05, with the field coils connected in parallel. The specification of the field coils is:

Inductance at 1kHz	25mH
Resistance at 20°C	14Ω
Peak-to-peak current for edge-to-edge scan at 25kV	875mA
Peak-to-peak current for 3% overscan at 25kV	900mA.

To counteract the increase in coil resistance with temperature, thermistor type VA1033 is included in the deflection coil assembly.

The timebase circuit is self-oscillating, with the flyback pulse on the anode of the PL508 applied to the grid of the ECC82. The circuit forms a multivibrator, the frequency of which is determined by the time-constant in the triode grid circuit. Interlace is very satisfactory.

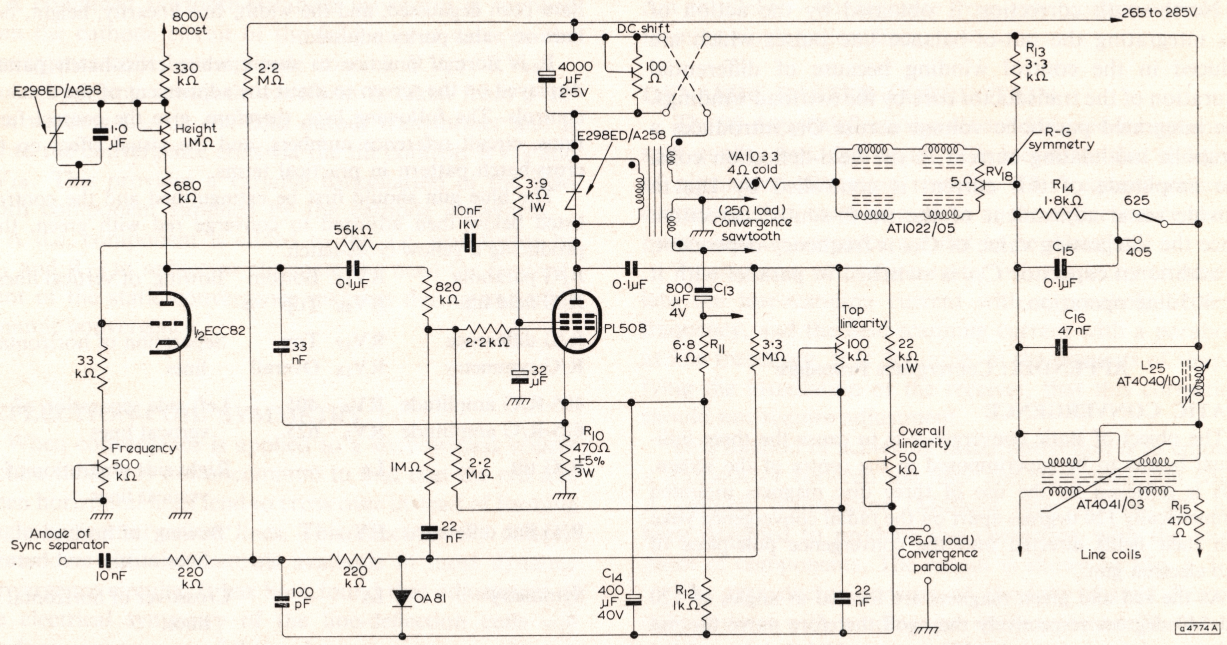

Fig. 2.1—Field timebase circuit for 90-degree colour tube: for complete field-convergence circuit see Fig. 1.3

Linearity

Linearity is effected by a conventional feedback network from the anode to the grid of the PL508. Cathode degeneration created by the convergence parabolic waveform taken from the cathode circuit, can give rise to some distortion at the bottom of the raster. This has been prevented by changing the earth points of the feedback network and cathode decoupling capacitor to the top of the 25Ω convergence parabola load. Synchronisation is achieved by applying a negative pulse to the grid of the PL508 via a diode gating network. The diode opens during flyback and closes during scan, thus preventing interference from reaching the grid of the PL508.

Deflection-coil Symmetry

By incorporating a potentiometer (RV_{18}, Fig. 2.1) in series with the two halves of the field-deflection coils, a field symmetry adjustment is provided. This adjustment can simplify the convergence of the top and bottom red and green horizontal lines, which would otherwise tend to run parallel to—but separate from—each other, instead of forming single yellow lines.

Pincushion Distortion Correction

The correction of pincushion distortion is effected by means of Mullard transductor type AT4041/03, in conjunction with a variable inductor type AT4040/10. These introduce an inductance of about 9mH and a resistance of 3·5Ω in series with the field coils. The effect of this extra loading has been taken into account in the design of the output transformer.

D.C. Shift

A decoupled variable resistor is included in series with the h.t. supply to the anode and the deflection coils, to provide a vertical shift. This is achieved with only a slight reduction in voltage swing (2V) from the transformer.

OUTPUT VALVE OPERATING CONDITIONS

The measurements recorded in Table 2.1 were carried out with a nominal PL508. The value of the cathode resistor was chosen to give the correct average anode current—that is, 57mA at a supply voltage of 265V. The height control was set for 3% overscan. Dissipation measurements were carried out with a cold transformer and with the d.c. shift control set to zero. The linearity controls were adjusted for 'zero initial slope' of the anode current waveform, and best linearity on the picture tube. The non-linearity was approximately 3%.

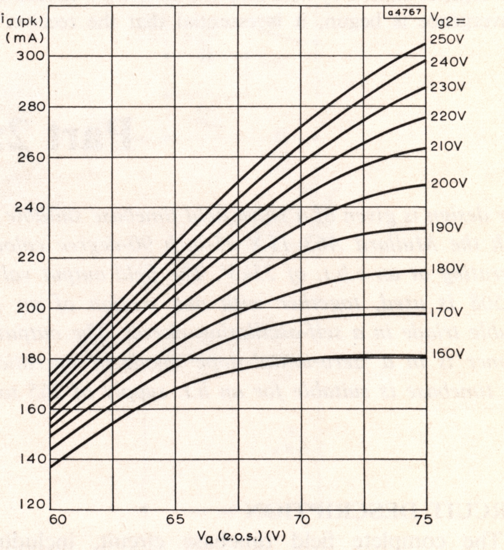

Fig. 2.2—Design chart for PL508 in stabilised field timebase Chart applies for h.t. of 240V. If h.t. is x volts, an amount (x—240)/10 should be added to anode potential at end of scan. An allowance of 10% is made for standing anode current.

TABLE 2.1: Operating Conditions of PL508

			Published data limits	
e.h.t.	25	25	—	kV
h.t.	265	285	—	V
V_{g2-k}	208	225	275max	V
V_k	22	23	—	V
I_k	65·9	71·6	100max	mA
I_a	57	62	—	mA
I_{g2}	8·9	9·6	—	mA
$i_{a(pk)}$	170	178	—	mA
$i_{a(o)}$	14	19	—	mA
$i_{a(pk-pk)}$	156	159	—	mA
$v_{a(pk)}$	945	965	2500max	V
$v_{a(e.o.s.)}$	65	85	62·5min	V
p_a	9·6	11·9	12·0max	W
p_{g2}	1·9	2·2	3·0max	W

TRANSFORMER SPECIFICATION

Laminations	E and I 'waste free' pattern MEA147
Grade	Silcor 25, Lamcor 4, Losil 25, etc. 0·4% silicon reannealed
Thickness	0·020in
Stack height	$\frac{7}{8}$in (square stack)
Former	S.R.B.P. tube; wall thickness, $\frac{1}{16}$in; length, $1\frac{9}{32}$in; internal dimensions, 0·95×0·95in minimum
Air gap	0·004in paper spacer each limb; that is, 0·008in total air gap in the magnetic path
Primary	2730 turns, 37 s.w.g. (0·173mm copper) Lewmex F enamelled copper wire, wound in 21 layers at 130 turns/layer
Interleaving	1 turn 0·002in paper/layer
Insulation	4 turns 0·002in paper
Convergence winding	64 turns 37 s.w.g. (0·173mm copper) tapped at 32 turns
Insulation	4 turns 0·002in paper
Secondary	300 turns 30 s.w.g. (0·315mm copper) Lewmex F enamelled copper wire in 4 layers at 75 turns/layer
Outer cover	1 turn 0·005in paper
Impregnation	Okerin 3700 wax
Build	85% with $\frac{1}{16}$in former
Cold resistances	Primary 230Ω Secondary 9·5 Ω. Convergence 6·6Ω total

Part 3: Shunt-stabilised Line Timebase

The design is given of a shunt-stabilised line timebase suitable for use with the Mullard A63–11X 25in 90-degree colour tube, operating at an e.h.t. of 25kV. The line output transformer is designed for 625- and 405-line operation. The stabilising circuit uses a voltage dependent resistor and a shunt triode. The design uses the desaturation technique and has a flyback ratio of 18%. Provision is made for balancing the line deflection coils, and a ±5% width control is incorporated. It is visualised that the convergence circuit will be at chassis potential and connected between two positions of the transformer winding feeding the deflection coils. The timebase is designed for ±10% mains variation.

INTRODUCTION

When conventional techniques are used for 90-degree deflection, difficulties arise in achieving third-harmonic tuning and in boosting the e.h.t. voltage sufficiently. These have led to a transformer design incorporating a large air gap which has meant a low L_s/L_y ratio and, consequently, a large VA requirement. A line transformer has therefore been designed using desaturation technique to scan the 90-degree colour picture tube at 25kV and, at the same time, to provide a well-stabilised e.h.t. up to 1·2mA.

In addition, the timebase will supply the requirements of the convergence circuits and other auxiliary services.

CIRCUIT DESCRIPTION

The circuit diagram of the line timebase is shown in Fig. 3.1. The design is based on the Mullard deflection coil type AT1022/05. The specification of the line coil is:

Inductance at 1kHz	2·9mH
Resistance at 20°C	2·8Ω
Peak-to-peak current for edge-to-edge scan at 25kV	2·74A.

Some departures from and additions to the conventional line timebase design are described below.

D.C. Shift

The d.c. shift through the deflection coils is obtained from the voltage developed across a 10Ω potentiometer connected to the cathode of the line output valve. A direct injection of the d.c. voltage into the deflection coil circuit is not possible because of the presence of the correction capacitor. For this reason it is fed through the a.c. blocking choke, L_1.

Third-harmonic Tuning

All the e.h.t. voltage is developed across winding 12–13 (which is placed on the opposite limb to the winding 1–9). Closer coupling is obtained by means of winding 10–11, which is inserted underneath the winding 12–13.

For 625-line operation, fine adjustment of the third-harmonic tuning is provided by adjustment of L_4. For 405-line operation, an additional series coil L_5 is brought into the circuit.

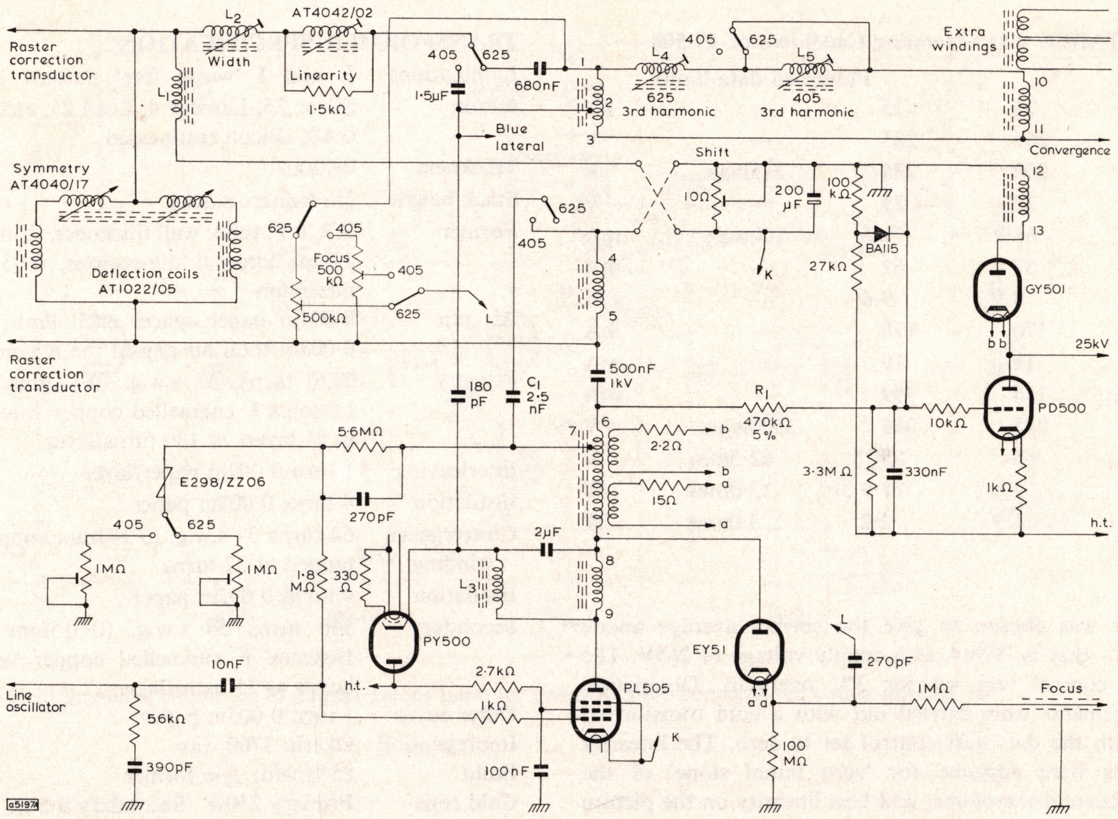

Fig. 3.1—Line timebase circuit

V.D.R. Stabilisation

A conventional circuit for v.d.r. stabilisation is used. Individual preset adjustments are employed for the two systems of operation. The circuit provides automatic adjustments for valve spreads and ageing, improves e.h.t. regulation, and makes the line timebase independent of mains variations. The present design covers $\pm10\%$ mains voltage variations for both systems.

Equalisation of scan is produced by connecting an extra flyback capacitor C_1 across part of the primary for 405-line operation.

Desaturation is achieved by passing the direct current from the diode through L_3 into the pentode. The booster diode is a.c. connected to the transformer by a 2μF capacitor.

A width control, consisting of a variable inductor L_2 in series with the line deflection coils, enables the scan to be varied by $\pm5\%$. The output stage is designed to give 9% overscan when L_2 is centre-positioned.

Shunt Stabiliser

For several reasons it is advantageous to operate the colour tube with as little e.h.t. variation as possible. Therefore a shunt stabiliser circuit is incorporated.

The line timebase is voltage-stabilised by means of a v.d.r. feedback loop. To minimise the interaction between the shunt stabiliser and the v.d.r. feedback circuit, it is necessary to operate the former in the 'constant-current' mode. In this mode, the shunt-regulator control voltage is obtained from across a resistor in series with the e.h.t. overwind. The operation of the circuit is such that the total e.h.t. load current is held constant. As the load contributed by the picture-tube beam current changes, the potential applied to the grid of the shunt regulator changes, causing the shunt regulator to draw an equal and opposite current.

A large amount of negative feedback is used, and this is sufficient to take care of any spreads in the PD500 and fall of emission during life. No setting-up controls are needed provided that resistor R_1 is of close tolerance (better than 5%). This resistor, together with the boost potential, provides a reference current for the stabilising circuit. The diode in the grid circuit prevents the grid-cathode potential from becoming excessive when the picture tube is heavily conducting; that is, when the shunt regulator is cut off.

Since the boost line is already stabilised by the action of the v.d.r. circuit, any voltage variation on the control grid of the shunt stabiliser results only from variation of the e.h.t. current through the e.h.t winding. Thus the circuit tends to maintain a constant current from the e.h.t. supply irrespective of the current drawn by the picture tube.

When the tube is cut off, the current flowing through the shunt stabiliser is set to 1·2mA. This does not imply that the maximum current drawn by the e.h.t. should not exceed this value. As shown by the e.h.t. regulation graphs in Fig. 3.2, the circuit still works when this value is exceeded, but with poorer regulation.

Similarly, if the mains variations exceed the quoted limits, the v.d.r. circuit may be out of control but the timebase still offers acceptable performance.

The heater of the shunt-stabiliser triode is intended to be connected in the series heater chain. Since its cathode warm-up time is shorter than that of the other valves, the circuit is ready for operation as soon as the e.h.t. becomes available, and in the event of a heater failure, the heaters are switched off.

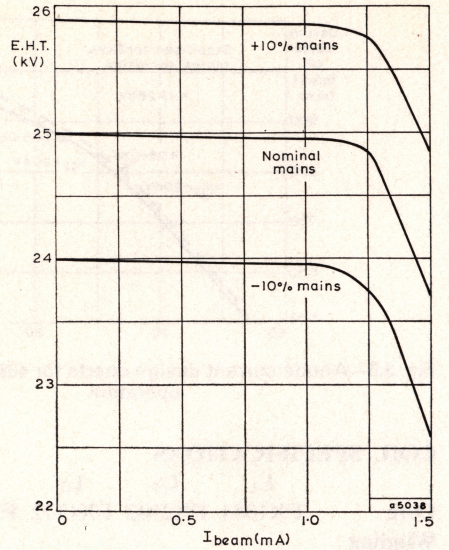

Fig. 3.2—E.H.T. regulation

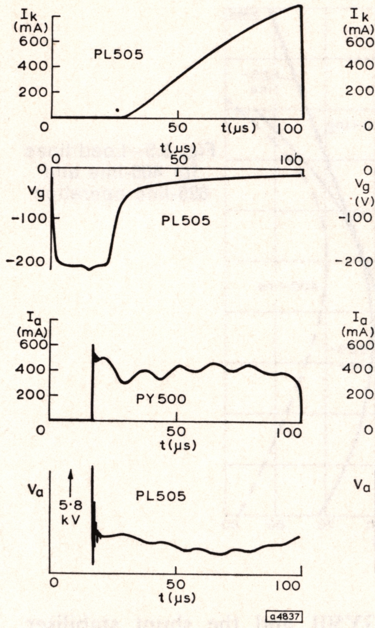

Fig. 3.3—Waveforms for 405-line operation

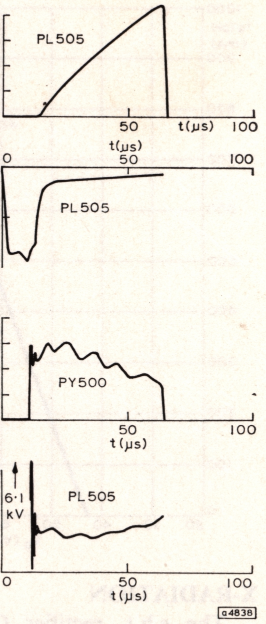

Fig. 3.4—Waveforms for 625-line operation

The absolute maximum permissible e.h.t. on the picture tube is 27·5kV. When the output stage is being adjusted to its correct performance, great care should be taken not to exceed this value in any circumstances.

Focus Supply

The focus supply voltage needed by the colour tube is derived by rectification of the high voltage pulses appearing at the cathode of the booster diode. Fine adjustment is made by varying the amplitude of the pulse applied to the 270pF reservoir capacitor by potentiometers connected between taps 1 and 5 of the line output transformer. With this method, a lower voltage exists between each focus potentiometer spindle and chassis.

Convergence Circuit Supply

The convergence circuit described in Part 1 has to be supplied with a negative-going sawtooth. To this end, the primary winding of the line output transformer is split at tap 3, one side being connected to the convergence circuit, the other side to chassis through the d.c. shift potentiometer.

A negative flyback pulse is taken from the 405-line coil (tap 2) to the blue lateral coil. An R/G symmetry coil has been added to the line deflection coils to assist R/G convergence.

Boost Line

The boost line has flyback pulses of about 750V superimposed upon the d.c. value. For this reason, any supply derived from the boost line must be smoothed by the insertion of a series impedance.

Oscillator

A flywheel oscillator employing the PCF802 valve is used. The output voltage is shaped by an R-C shaping network.

Pentode Waveform

The ratio of magnetic energy to losses and, therefore, the ratio of peak-to-average anode current, is not very favourable for a 90-degree colour line timebase. In a line timebase, the output valve must be cut off for a period longer than the flyback time, which gives a theoretical minimum value of the ratio $i_{a(pk)}/I_a$ as $1/(1-p)$, or 1·22. The actual value of this ratio is determined by the type of oscillator used. The minimum value realisable with a sinewave oscillator using a PCF802 is about 1·6.

In the present design, the required peak anode current is about 550mA, and the average current is about 370mA. With this ratio of 1·5 and the value of I_a of 370mA, the waveform of $i_{a(pk)}$ has to be very rectangular in shape. This is reflected in a large sag in the pentode anode voltage. To achieve a better $i_{a(pk)}/I_a$ ratio, and therefore to reduce this sag in the anode voltage, the $i_{a(pk)}$ waveform should be more triangular in shape. The value of $i_{a(pk)}$ is increased by about 250mA by a control-grid shaping network, and this is reflected in an increase in the booster diode current at the end of scan of approximately the same magnitude.

The anode voltage and cathode current waveforms are shown in Figs. 3.3 and 3.4. From these results the load lines can be drawn, and these are shown in Fig. 3.5. To a first approximation, it can be assumed that the I_a/V_a characteristic below the knee can be represented by a straight line passing through zero. If valve and component spreads of 15V and a $\pm10\%$ mains voltage variation at 285V are taken into account, the locus of anode potential at the end of scan can also be drawn as a straight line parallel to the below-the-knee characteristic, moved 43V to the right. The end-of-scan voltage is purposely put at a higher level to ensure that the entire load line characteristic is situated to the right of the line for the end-of-scan voltage. The load line will therefore still be above the knee at -10% mains voltage and adverse component spreads.

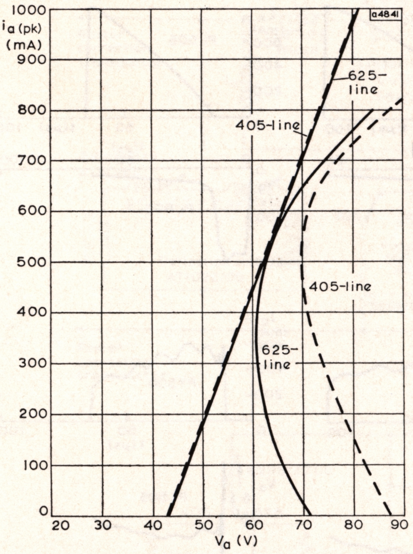

Fig. 3.5—Load lines for 405-line and 625-line operation

X-RADIATION

The e.h.t. rectifier GY501 and the shunt stabiliser PD500 used in this circuit emit x-rays well in excess of the permissible dose rate. Suitable x-radiation screening must therefore be provided at all times.

VALVE OPERATING CONDITIONS

The measurements recorded in Table 3.1 were carried out with nominal valves and with the transformer which also supplies necessary drain from the boost line for the field oscillator and from the extra windings (flywheel, a.g.c. and so on).

The e.h.t. regulation curves are given in Fig. 3.2; waveforms for the PL505 and PY500 in Figs. 3.3 and 3.4; anode current design charts in Fig. 3.6.

TABLE 3.1

Operating Conditions of PL505 and PY500

	625-line	405-line	Published limits	
h.t.	285	285	—	V
I_b	1·2	1·2	—	mA
PL505 (screen-grid resistor 2·7kΩ; decoupling capacitor 0·1μF)				
$v_{a(pk)}$	6·1	5·8	7max	kV
I_a	360	345	—	mA
I_{g2}	30	30	—	mA
$i_{k(pk)}$	880	900	—	mA
$i_{g2(e.o.s.)}$	80	80	—	mA
$i_{a(pk)}$	800	820	—	mA
V_{g2}	204	206	—	V
$v_{a(e.o.s.)}$	84	90	—	V
p_a	24·3	24·7	25max	W
p_{g2}	6·1	6·2	7max	W
PY500				
$v_{a-k(pk)}$	4·4	4·2	5·6max	kV
$i_{a(pk)}$	610	500	800max	mA
I_a	360	345	440max	mA
v_{boost}	820	800	—	V
Flyback time	11·5	17·8	—	μs

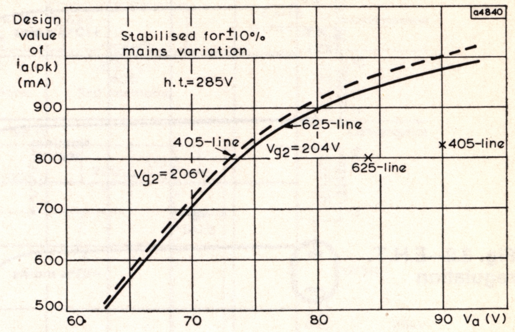

Fig. 3.6—Anode current design charts for 405-line and 625-line operation

COIL SPECIFICATIONS

	L_1	L_2	L_3	L_4	L_5
Core	FX1054	FX2142	FX1172	FX1054	FX1054
Winding					
turns	800	150	500	400	300
turns/layer	100	50	100	100	80

All windings, 30 s.w.g. Simms QSE.

LINE OUTPUT TRANSFORMER SPECIFICATION

Core	FX2935 and FX2936
Air gap	2×0·003in paper
Former for winding 1–9	S.R.B.P., I.D. $\frac{3}{4}$in, wall $\frac{1}{32}$in
Former for winding 10–13	S.R.B.P., I.D. $\frac{3}{4}$in, wall $\frac{1}{32}$in
Winding 1–9	440 turns 27 s.w.g. (0·417mm) Simms QSE would at 48 turns/layer tapped at 32, 48, 145 and 340 turns
Winding 10–11	68 turns 30 s.w.g. (0·315mm) Simms QSE wound at 35 turns/layer
Winding 12–13	1680 turns 40 s.w.g. (0·122mm) Simms QSE wound at 30 turns/layer
Winding a–a	2 turns of suitably insulated wire
Winding b–b	2 turns of suitably insulated wire
Interleaving	
Winding 1–9	2×0·003in paper between each layer
Winding 10–11	2×0·004in cellulose acetate butrate foil between each layer
Winding 12–13	2×0·004in cellulose acetate butrate foil between each layer
Between windings 10–11 and 12–13	4×0·004in cellulose acetate butrate foil
Impregnation	Okerin 3700 wax, immersion for 2 hours

Winding positions are given in Fig. 3.7.

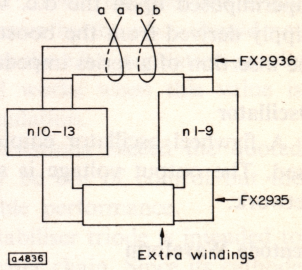

Fig. 3.7—Position of coils on Ferroxcube core